(D) REMARKS, including DRAWING AMENDMENTS, if any

The issue is whether under Sec. 103 the Alter invention is obvious in view of U.S. Pat. No. 6,734,093 (Sabin et al.) combined with U.S. Pat. No. 6,255,737 (Hashimoto).

The law is clear. In Ex parte Levengood, 28 USPQ2d 1300, the Board of Patent Appeals and Interferences stated (emphases added):

> "In order to establish a prima facie case of obviousness, it is necessary for the examiner to present *evidence*, preferably in the form of some teaching, suggestion, incentive or inference *in the applied prior art*, or in the form of generally available knowledge, that one having ordinary skill in the art would have been led *to combine the relevant teaching of the applied references in the proposed manner to arrive at the claimed invention.*"

Applicant Alter has defined and claimed specifically "...wafer-level packaging including an electrically conductive material beam...." Claim 1. Alter in his Background section clearly describes known manner "wafer-level packaging" (WLP) and sets his intentions at "...further discoveries in this regard." (Page -4-, line 9-10). More specifically, Alter is providing for "...*integration* of WLP bump-out beans into IC [integrated circuit] device elements." (Page -5-, lines 5-6; claims 1-11).

The allegations of the Action, and the cited references alone or in combination, fail to meet any of the criteria as described in Levengood for the following reasons.

The Action, at page 4, starting at line 3, alleges,

> "Sabin et al. teach *forming an active circuit beneath* a metallization structure including bonding pad metal layer/*CMB [conductive beam material]*...".

First, Sabin provides no evidence for the propositions asserted in the Action. The Office admits that there is no "...integration of WLP bump-out beams into IC device elements." See Alter claim language, *supra*. The latter reference in the allegation to conductive beam material "CMB" is an extrapolation; it is not anywhere to be disclosed by, nor even remotely suggested by Sabin et al. themselves. In their own words, Sabin et al. only describe:

> "The present invention provides a *bonding pad structure* for integrated circuit devices which allows the *active circuits* to be placed *under bonding pads* of the device without affecting the performance of the active circuits." Abstract (emphases added);
>
> "...design of a bonding pad structure..." Col. 1, ll. 7-8.

The problem and purpose, again described in Sabin et al. own words is,

> "...so that the bonding pad may be subjected to *thermal and mechanical stresses without damaging the underlying active circuits*." Abstract (emphasis added);"

and

> "The present invention enables a reduction in the chip area and *eliminates the parasitic resistance due to long interconnection wires* between bonding pads and active regions." Abstract (emphasis added);"

and

> "Bonding pads are generally not located above the active circuits in order *to protect the active circuit elements during bonding processes*." Col. 1, ll. 27-29;

and

"...desirable to place active circuits *beneath* the bonding pads." Col. 1, ll. 30-31;

"Therefore, what is needed is a method for fabricating a bonding pad structure which allows the placement of active circuits beneath a bonding pad, without damaging or otherwise affecting the performance of the active circuits, ..." Col. 1, ll. 45-48.

Sabin goes on to describe an "...*underlying structure* over which a bonding pad may be formed." Col. 2, ll. 37-38.

Thus, even a cursory referral to Sabin et al. proves *by its own words* that it is neither directed to the same problem nor the same purpose as Alter and that, more over, they *never considered "wafer-level packaging" structures nor methods at all.* There are many other such admissions by Sabin et al. proving its irrelevancy and its failure as "evidence" against the present application; if not withdrawn, applicant reserves the right to argue with respect to those passages also.

The Action goes on to state that,

"Furthermore, the metallization structure includes a conventional capacitor structure having the bonding pad metal layer/first plate and a metal layer/second plate separated by a dielectric layer [Sabin et al. citation]." Page 4, first full para., last sentence.

Yet, in Sabin et al.'s *own words* they are describing:

"...the *underlying structure* over which a bonding pad may be formed. ***...*helps absorb compressive stress and insulates from thermal stress during the bonding process.*" Col. 2, ll. 37, 53-55 (emphasis added).

In other words, in Sabin et al.'s own words there is no such alleged "conventional capacitor structure" at all. This is a blatant redefinition of the actual teaching of Sabin et al. to meet the argument propounded in the Action.

Clearly, given the actual description in Sabin et al.'s own words, the only reason for considering Sabin et al. at all is to try to build something to defeat the present application given Alter's teachings. This is not appropriate. Hindsight reasoning using the invention for which a patent is sought as a template is impermissible. Texas Instruments, Inc. v. ITC, 26 USPQ2d 1018 (CA FC 1993).

Sabin et al. by its own words fails to stand for propositions asserted to bolster the Action's arguments. No reference combined with it can thus support an overall allegation. It is therefore requested that the rejections be withdrawn on this ground.

Moreover, in order to further prosecution, applicant also notes that the combination of Sabin et al. with Hashimoto relied upon by the Office similarly fails to teach, motivate or suggest the Alter invention. The combination fails for the following reasons.

Hashimoto is concerned with chip size packing, acknowledging it to be known in the art (Col. 1, ll. 14 -18) as does Alter (see Background). Hashimoto's problem and purpose is clearly defined in his own words,

> "...apart from the stress absorbing layer, thermal stress can be effectively absorbed." Col. 1, ll. 34-35."

Hashimoto goes on throughout the patent in his own words describing methods and structures to the thermal stress problem. Again, this has nothing to do with the invention described and claimed by Alter.

In fact, for the purpose of argument, even had Sabin et al. stood for the propositions asserted by the Action, the combination of Sabin et al. with Hashimoto via their own direct words would lead logically to:

> a *dual level bonding pad with active elements beneath them also having bump out wafer-level packaging with improved thermal stress resistance*.

This *prima facie* is not the invention described nor claimed by Alter.

The combination of Sabin et al. and Hashimoto failing to stand for the propositions asserted, it is again respectfully requested that the rejections be withdrawn.

SUMMARY AND CONCLUSIONS

Alter teaches in claims (1-11, Group I as elected), novel, non-obvious uses and improvements for wafer-level packaging and active IC components integrated directly into elements of the wafer-level packaging. The references cited are irrelevant and immaterial to all Alter's claims. Based upon the foregoing, it is submitted that the application now presents claims which are directed to novel, unobvious and distinct features of the present invention which are an advancement to the state of the art. Reconsideration and early allowance of all claims is respectfully requested. The right is expressly reserved to reassert any and all arguments, including the raising of new arguments, should a Notice of Allowance not be forthcoming.

Questions or suggestions that will advance the case to allowance may be directed to the undersigned by teleconference at the Examiner's convenience.

Date: SEPT. 8, 2004

Respectfully submitted,
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